REMARKS

Claims 9-20 are currently active.

Claims 1-4 and 6-8 have been canceled.

The Examiner has rejected Claims 1-4 and 9-20 as being anticipated by Chao. Applicants respectfully traverse this rejection.

Chao teaches a storage means is provided with M locations, one for each of a number of timestamps. In each of the locations a validity bit is stored. If the validity bit is "1", it will include a pointer to a linked list of identifiers of flow queues having a head of line packet with a corresponding timestamp. Chao teaches to use a hierarchical searching technique to find the first memory location with a validity bid of "1". See column 21, lines 1-10.

Chao teaches a packet scheduler. The packet scheduler may be located at each of the output ports of the switch or router. A CPU computes timestamps and other system control. Packets are associated with addresses defined by their timestamps and may be stored in memory. The next packet search engine selects the next head of line packet to be

transmitted over the transmission medium coupled at the output port. See column 22, lines 36-46.

Chao teaches that first, a search is performed to find the flow queue with a head of line packet having a lowest timestamp. Next, it is determined whether any more head of line packets have the same timestamp. If not, the validity bit is reset. Further, since the bits and strings and higher levels in the hierarchy may be affected by the change of the validity bit, these bits are also reset, if necessary. If there are more packets with the timestamp, then the validity bid remains 1 and there are no changes. Next, It is determined whether there is a new head of line packet and a flow queue. This will occur at a flow queue having more than one packet in which the head of line packet is serviced. When searching for the flow queue with a head of line packet having the lowest timestamp, the hierarchical level is set to zero. Next, the contents of the register are encoded to generate a bit string. If the level is not greater than a maximum level, a RAM at the current level is read, using an address defined by encoded bit strings. The read contents of the RAM are encoded, to generate a bit string.

Next, the most significant bits of the binary coded timestamp are extracted. Next, the contents of memory at the next level address using the extracted bits, are read. In addition, the decoded word of the extracted bits and the contents of the memory at level 0 are logically Or'd. The result is written back to the memory at level 0. Additional bits are

extracted from the binary coded timestamp and these additional extracted bits are decoded to generate an additional bit decoded word. The additional decoded word and the contents of the memory at level 1 are logically ordered, bit by bit, to generate a result which is written to the memory at the next level, addressed by the decoded word. See column 23, lines 1-67.

In regard to Claim 16 of applicants, there is the limitation "the first memory comprising at least 2 linear time indexed arrays having a plurality of locations, at least one of the 2 linear time indexed arrays configured to buffer at least one first data unit". As explained above, Chao does not teach or suggest 2 linear time-indexed arrays having a plurality of locations.

Furthermore, there is a limitation in Claim 9 of "indicating with a variable there is a valid data unit in the respective location". There is no teaching or suggestion at all in Chao of a variable that indicates if there is a valid data unit in a respective location. Chao does not teach or suggest whether the data unit is valid or not. Accordingly, Chao does not anticipate claim 9. Claims 10-15 are dependent to parent Claim 9 and are patentable for the reasons Claim 9 is patentable. Claim 16 is patentable for the reasons Claim 9 is patentable. Claims 17-20 are dependent to parent Claim 16 and are patentable for the reasons Claim 16 is patentable.

The Examiner has rejected Claims 6 and 8 as being unpatentable over Gritton in view of Chao. Applicants respectfully traverse this rejection. Claims 6 and 8 have been canceled.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 9-20, now in this application be allowed.

Respectfully submitted,

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